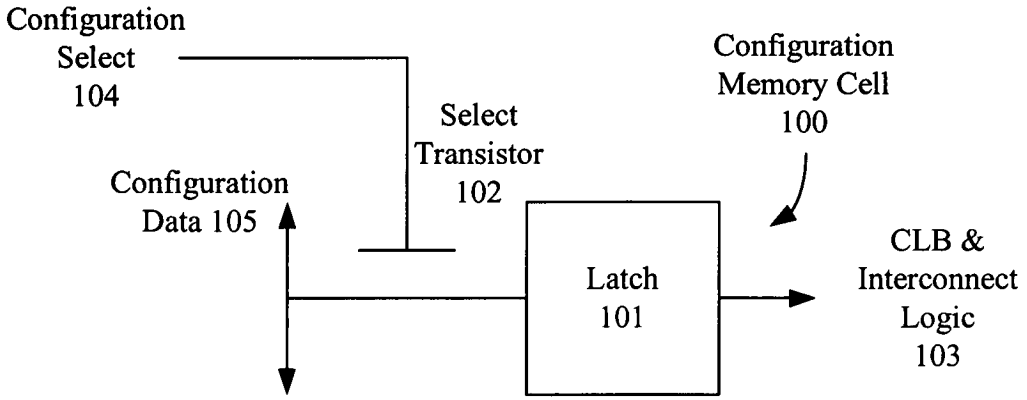

Figure 1
(Prior Art)

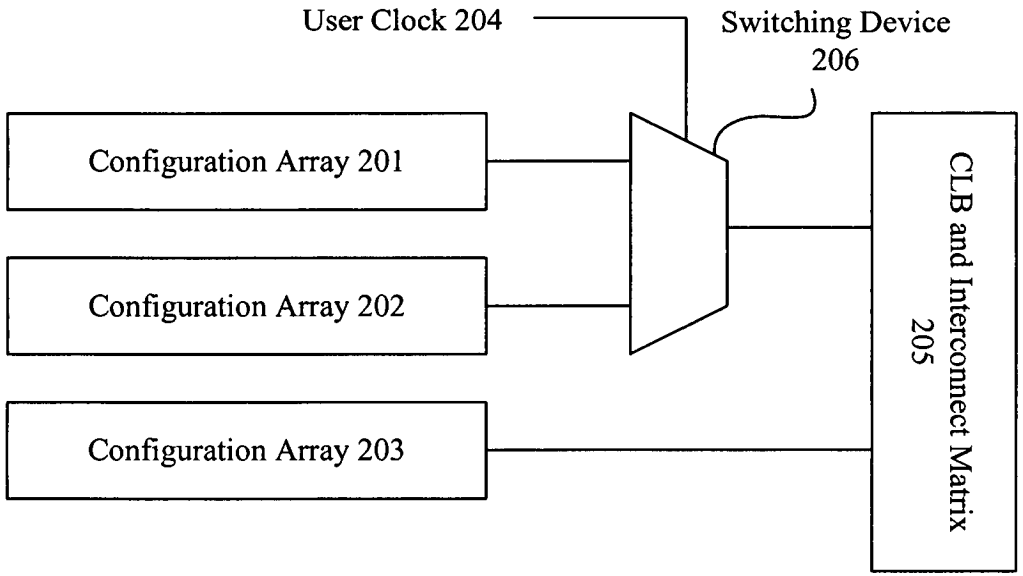

Figure 2

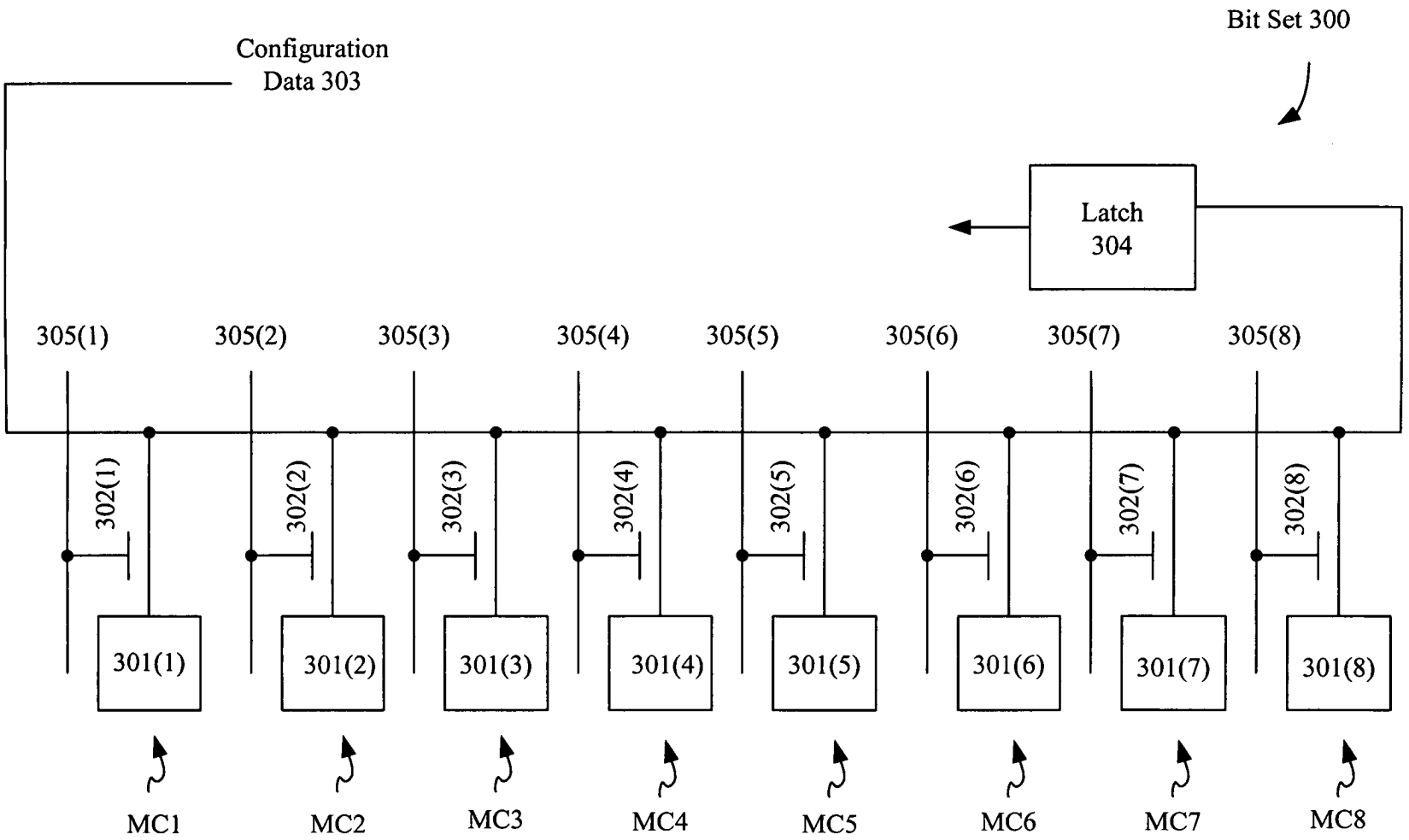
Bit Set 300
Configuration Data 303
Latch 304
305(1)
305(2)
305(3)
305(4)
305(5)
305(6)
305(7)
305(8)
302(1)
302(2)
302(3)
302(4)
302(5)
302(6)
302(7)
302(8)
301(1)
301(2)
301(3)
301(4)
301(5)
301(6)
301(7)
301(8)
MC1
MC2
MC3
MC4
MC5
MC6
MC7
MC8

Figure 3

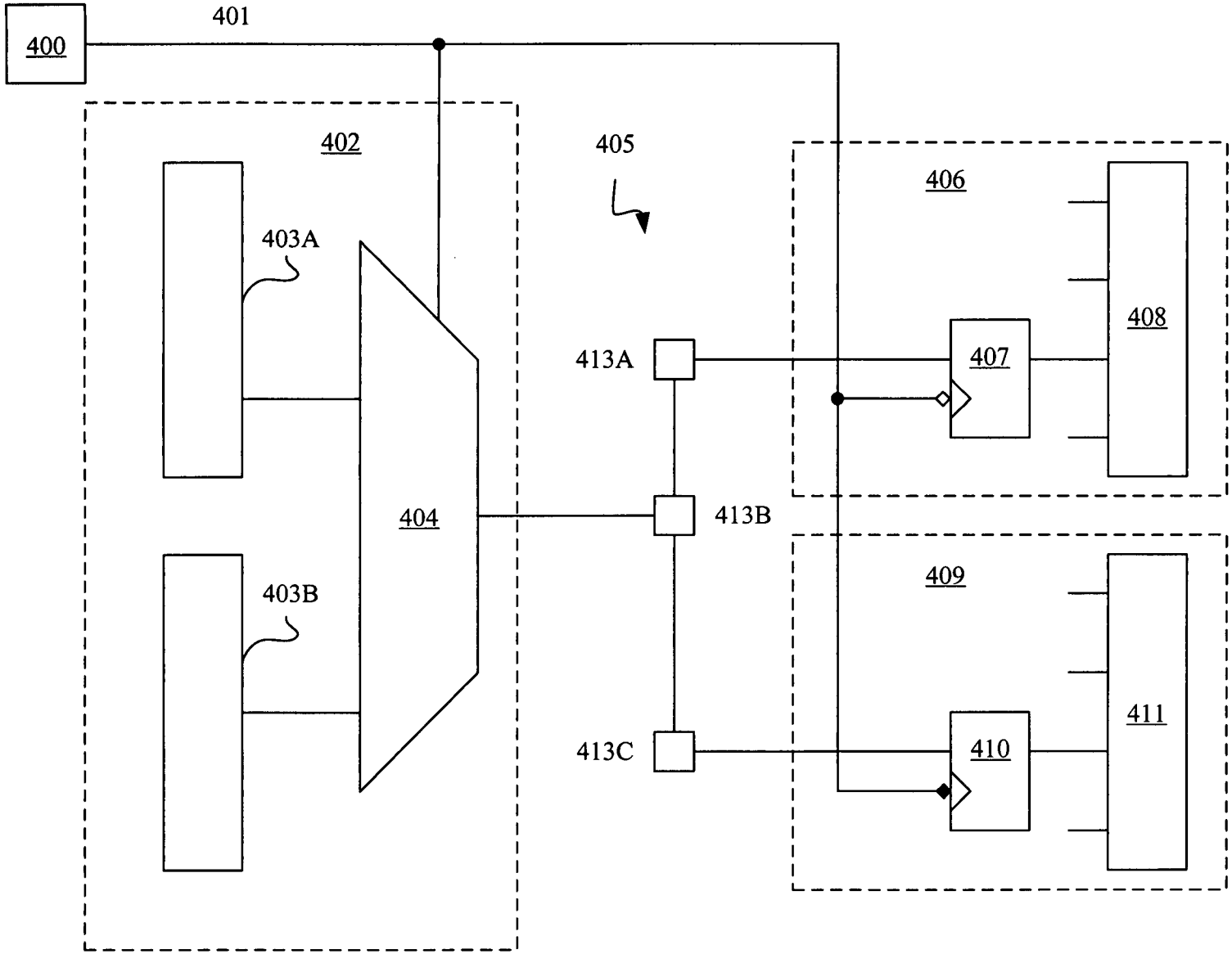
400
401
402
403A
403B
404
405
406
407
408
409
410
411
413A
413B
413C

Figure 4A

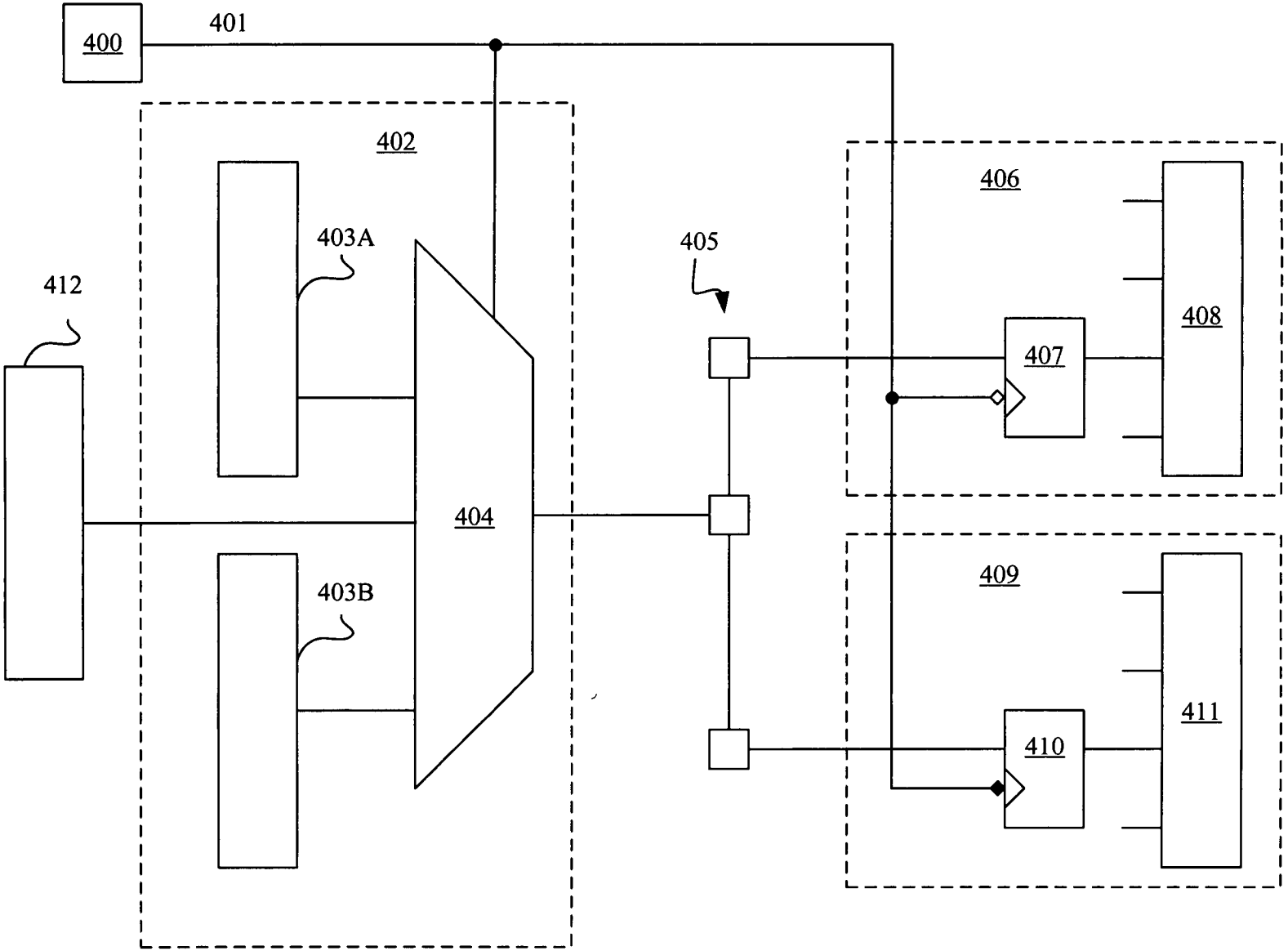

Figure 4B

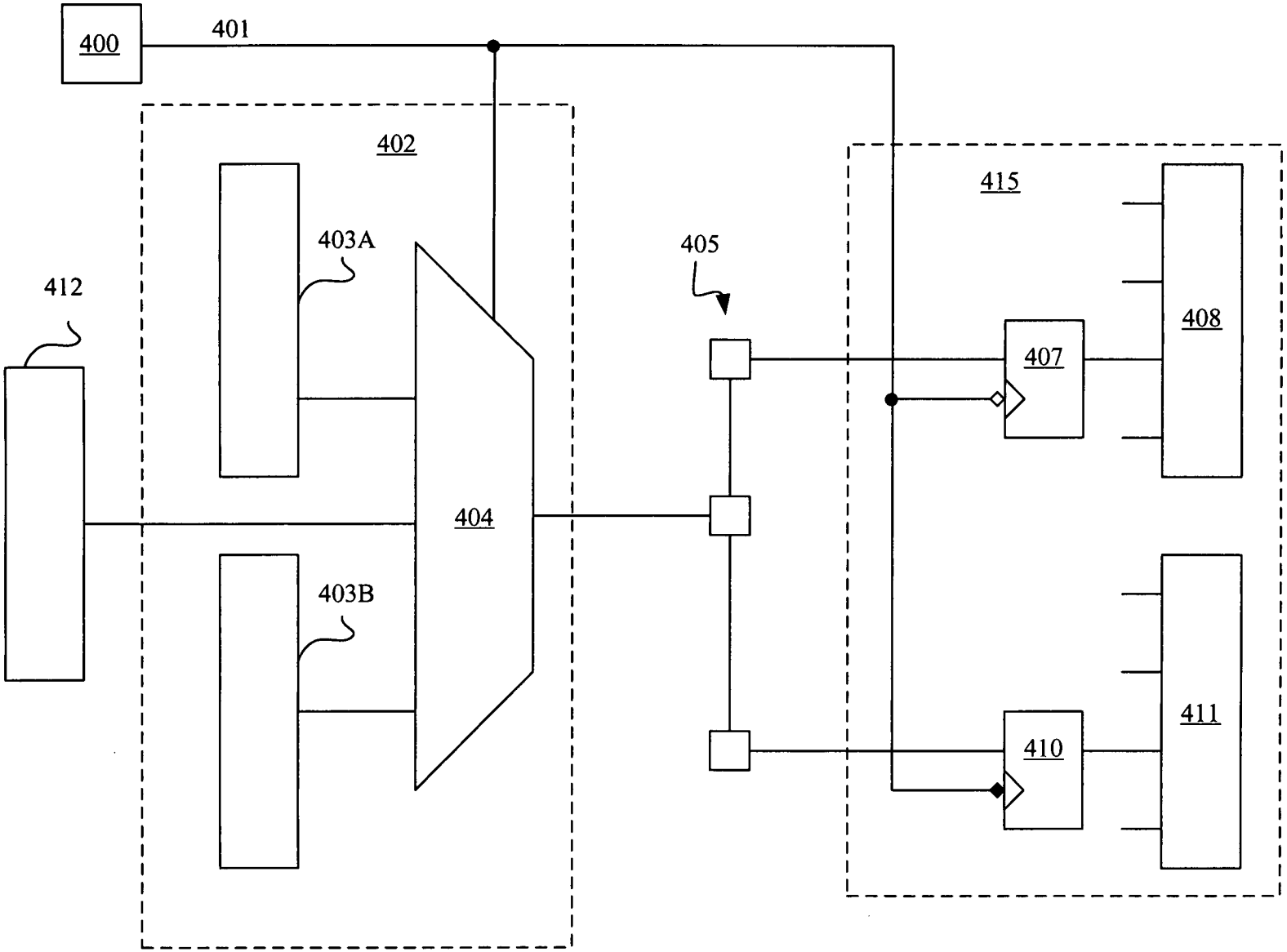

Figure 4C

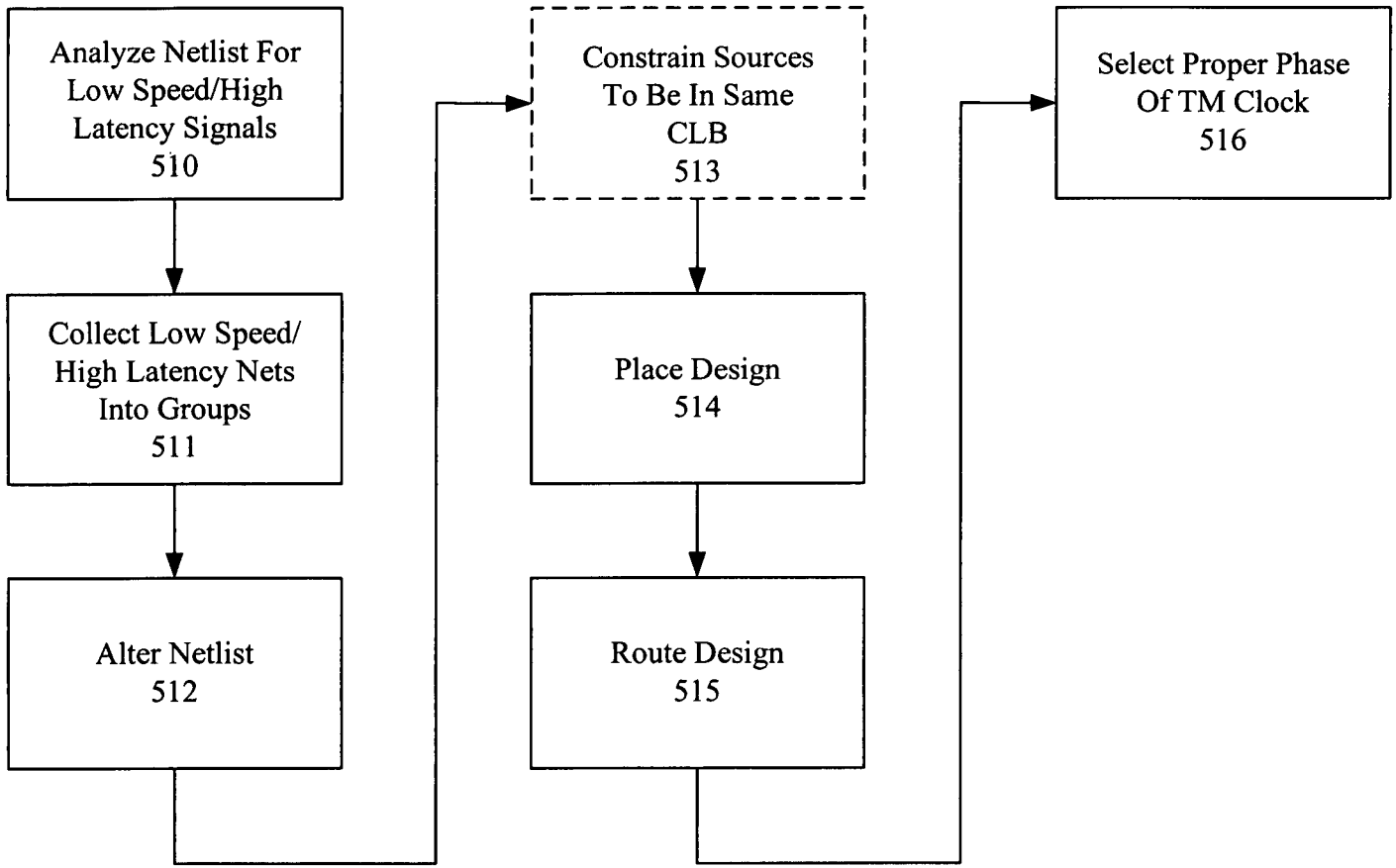
Analyze Netlist For Low Speed/High Latency Signals 510
Collect Low Speed/ High Latency Nets Into Groups 511
Alter Netlist 512
Constrain Sources To Be In Same CLB 513
Place Design 514
Route Design 515
Select Proper Phase Of TM Clock 516

Figure 5A

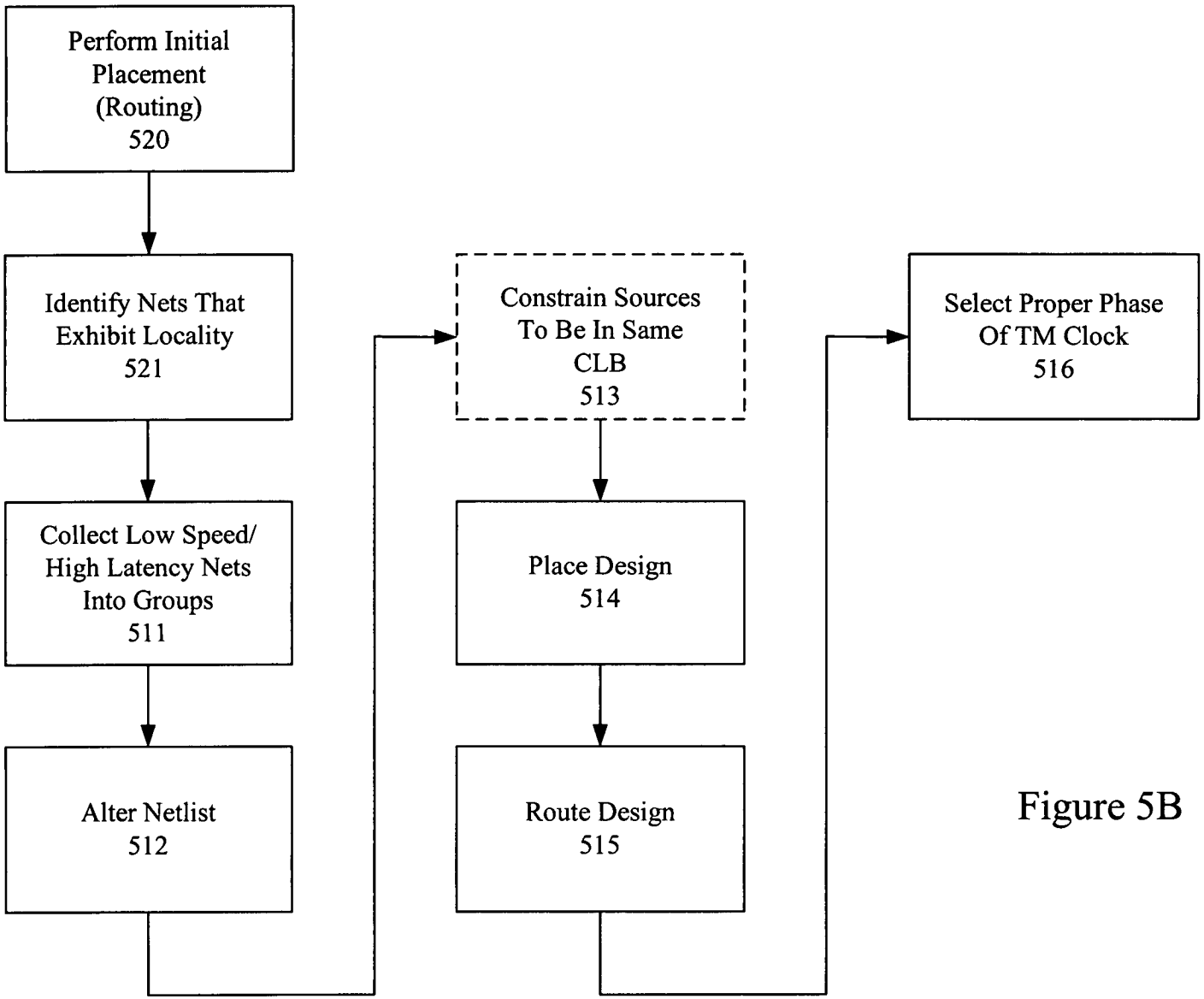
Perform Initial Placement (Routing) 520
Identify Nets That Exhibit Locality 521
Collect Low Speed/ High Latency Nets Into Groups 511
Alter Netlist 512
Constrain Sources To Be In Same CLB 513
Place Design 514
Route Design 515
Select Proper Phase Of TM Clock 516

Figure 5B

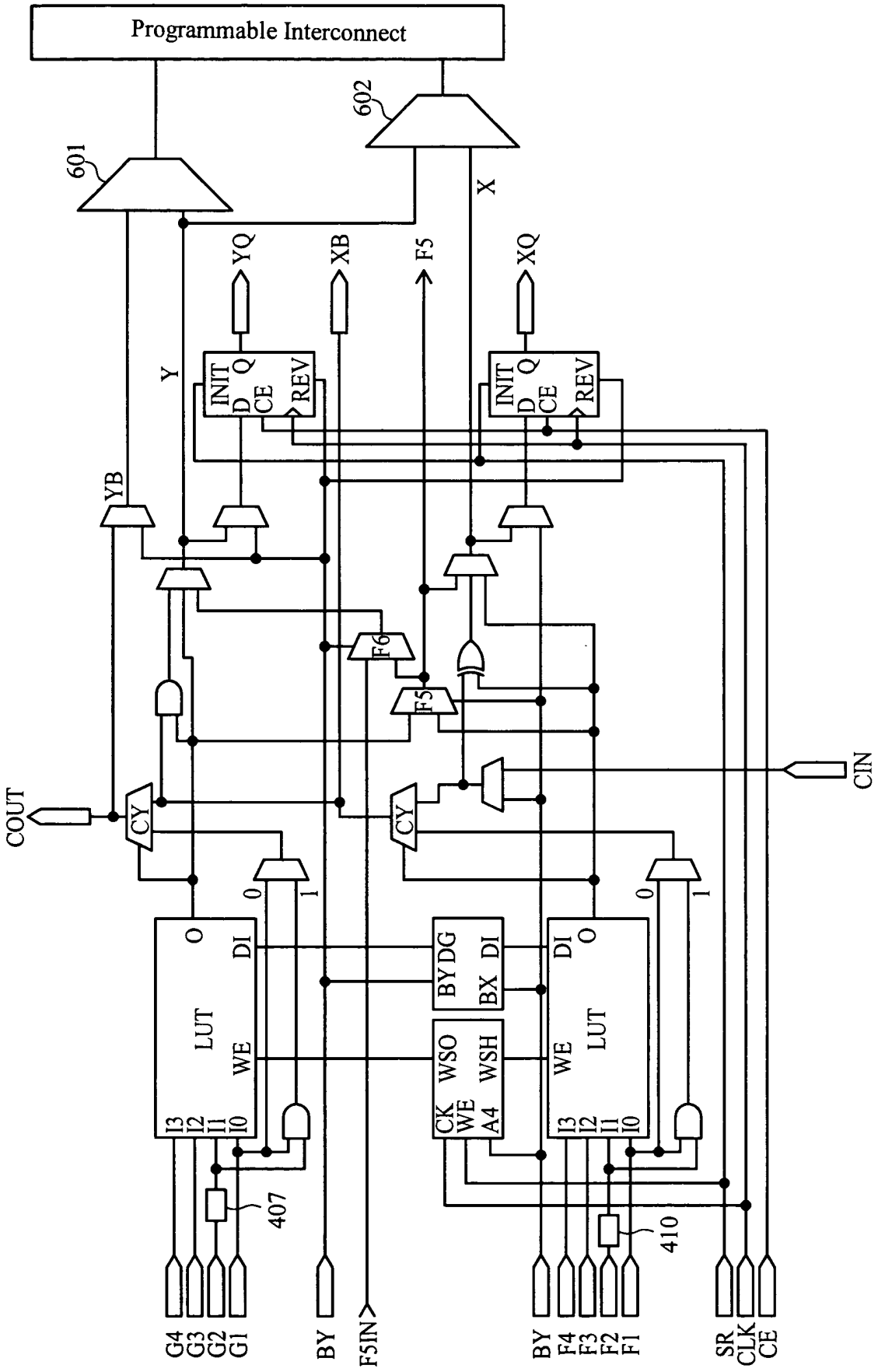
Programmable Interconnect
601
602
X
Y
YQ
XB
F5
XQ
INIT
D
Q
CE
REV
YB
F6
F5
COUT
CY
CIN
O
DI
LUT
WE
I3
I2
I1
I0
BYDG
BX
WSO
WSH
CK
WE
A4
407
410
G4
G3
G2
G1
BY
F5IN
F4
F3
F2
F1
SR
CLK
CE

Figure 6